REMARKS

In response to the non final Office Action dated February 28, 2003, applicant hereby makes the following response. Claims 1-8 were originally pending with claims 1 and 8 being independent. In an earlier response, claims 1-8 were cancelled and new claims 9-28 were added with claims 9, 15 and 21 being independent. In the final Office Action, the Examiner withdrew claims 15-28 as subject to a restriction requirement. In an additional response, claims 13 and 14 were cancelled. In this response, claim 9 is being amended and claim 10 is being cancelled.

Rejection Under 35 U.S.C. § 112

Claim 10 stand rejected under 35 U.S.C. 112, second paragraph, as allegedly indefinite for failing to particularly point out and distinctly claim the subject matter. Claim 10 has been cancelled.

Rejection Under 35 U.S.C. § 102(b)

Claims 9-12 stand rejected under 35 U.S.C. 102(b), as being allegedly anticipated by *Kuroda et al.* (U.S. Patent No. 5,479,138). Claim 9 has been amended to further define the structure of the invention. The present invention teaches that the conductive pattern (the signal pattern) is formed in the inside layer in the dielectric substrate. Further, the earthed conductor pattern is formed on the surface of the dielectric substrate wherein the dielectric substrate has one or plural areas without the earthed conductor. Accordingly, the earthed conductor pattern is exposed for convenient processing. Thus, the frequency characteristic of the circuit device can be changed by positioning conductive parts on the areas free of the earthed conductor to narrow the frequency. The frequency characteristic may also be changed by sizing the lattice pattern to widen the frequency.

Applicant respectfully notes that the *Kuroda et al.* reference does not teach a circuit device wherein the earthed conductor is formed on the surface of the dielectric substrate in a lattice pattern (see specification page 4, lines 18-23.) Instead, *Kuroda* teaches the conductor in the insulation layer (see Fig. 1B, elements, G1 and G2). Accordingly, in *Kuroda*, the earthed conductor is not exposed on the surface prohibiting any access for processing. Additionally, the *Kuroda et al.* reference does not teach a lattice pattern having areas free from the earthed conductor (see specification page 7, lines 24-30, page 8, lines 6-14, page 9, lines 14-26).

Applicant respectfully submit that the *Kuroda et al.* reference does not anticipate the present invention as claimed for at least these reasons. Applicant respectfully submits that since Claim 9 is patentable, all dependent claims therefrom are also patentable.

CONCLUSION

The Applicant respectfully requests withdrawal of the rejection and believes that the Claims as presented represent allowable subject matter. However, if the Examiner desires, the Applicant's attorney is ready for a telephone interview to expedite prosecution. As always, the Examiner is free to call the undersigned at 312-876-7518.

Respectfully submitted,

SONNENSCHEIN NATH & ROSENTHAL

5/13, 2003

By: Brian J. Gill

Brian J. Gill
Reg. No. 46,727

SONNENSCHEIN NATH & ROSENTHAL
P.O. Box 061080
Wacker Drive Station - Sears Tower
Chicago, IL 60606-1080
(312)876-8000

I hereby certify that this document and any being referred to as attached or enclosed is being deposited with the United States Postal Service as first class mail in an envelope addressed to Mail Stop Non-Fee Amendment, Comm. For Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on

5/13/03 Paula M. Theismann
Date Paula Theismann

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re U.S. Patent Application of: T. Hirabayashi

Serial No.: 09/641,206

Filed: August 18, 2000

For: CIRCUIT DEVICE AND PRINTED CIRCUIT BOARD

Examiner: S. Jones

Group Art Unit: 2817

Attorney Docket No. 9792909-0398

Mail Stop Non-Fee Amendment
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

VERSION TO SHOW AMENDMENTS MADE

9. (Second Amendment) A circuit device, comprising:

a dielectric substrate, the dielectric substrate having a first area and a second area;

at least one conductive pattern formed in the first area; and

at least one earthed conductor formed on the surface of the second area, the at least one earthed conductor being formed in a lattice pattern on the surface of the second area wherein the lattice pattern has areas free of the at least one earthed conductor.

14283122v1